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Claims

[c1] 1.A varactor, comprising:
a semiconductor material having a continuous column with a lower region, a middle region, and an upper region, wherein:
a first dopant is disposed in the lower region of the continuous column;
a second dopant is disposed in the middle region of the continuous column; and
a third dopant is disposed in the upper region of the continuous column.

[c2] 2.The varactor of claim 1, wherein a majority of the first dopant is disposed in an area centered about 1 μm below the top of the continuous column of semiconductor material.

[c3] 3.The varactor of claim 1, wherein the lower region defines a cathode, the middle region defines a hyper-abrupt junction, and the upper region defines an anode.

[c4] 4.The varactor of claim 1, wherein the lower region is comprised of a bottom layer and an upper layer, wherein the bottom layer has a higher concentration of first

dopant than the upper layer.

[c5] 5.The varactor of claim 4, wherein the upper layer defines a collector.

[c6] 6.The varactor of claim 1, wherein the upper region is substantially planar with an upper surface of the semiconductor material, the upper surface of the semiconductor material including at least one insulation region disposed on a side of the continuous column.

[c7] 7.The varactor of claim 1, wherein the first dopant comprises a first N-type dopant, the second dopant comprises a second N-type dopant, and the third dopant comprises a P-type dopant.

[c8] 8.The varactor of claim 7, wherein:
the first dopant comprises at least one of phosphorus, arsenic, and antimony;
the second dopant is different from the first dopant and comprises at least one of phosphorus, arsenic, and antimony; and
the third dopant comprises at least one of boron, gallium, and indium.

[c9] 9.The varactor of claim 1, further comprising at least one isolation region adjacent to the continuous column and above a bottom layer of the lower region of the continu-

ous column.

[c10] 10.The varactor of claim 1, further comprising at least one reach-through implant in electrical communication with the lower region defined as a cathode region.

[c11] 11.A hyper-abrupt junction varactor, comprising:
a substrate having a subcollector region and a plurality of isolation regions;
a first region of a first conductivity type is provided adjacent the subcollector region between at least a pair of the plurality of isolation regions; and
a second region of a second conductivity type which is different from the first conductivity type being located adjacent the first region and between the at least pair of the plurality of isolation regions.

[c12] 12.The hyper-abrupt junction varactor of claim 11, wherein the second region is located in a layer of the substrate.

[c13] 13.The hyper-abrupt junction varactor of claim 11, wherein the first dopant region is N-type doped and the second dopant region is P-type doped.

[c14] 14.The hyper-abrupt junction varactor of claim 11, further comprising:
a third region of the first conductivity type having a

dopant concentration lower than a dopant concentration of the first region and the second region, the third region located in the substrate beneath the first and second regions.

[c15] 15.The hyper-abrupt junction varactor of claim 14, wherein the first and third region comprises antimony.

[c16] 16.A method of fabricating a varactor, comprising:
providing a semiconductor substrate;
doping a lower region of the semiconductor substrate with a first dopant;
doping a middle region of the semiconductor substrate with a second dopant; and
doping an upper region of the semiconductor substrate with a third dopant.

[c17] 17.The method of claim 16, further comprising forming a cathode of the varactor in the lower region, forming a hyper-abrupt junction in the middle region, and forming an anode in the upper region.

[c18] 18.The method of claim 16, further comprising forming the first dopant from a first N-type dopant, forming the second dopant from a second N-type dopant, and forming the third dopant from a P-type dopant.

[c19] 19.The method of claim 16, further comprising doping a

bottom layer of the lower region with a higher concentration of the first dopant than an upper layer of the lower region.

[c20] 20.The method of claim 19, further comprising forming a collector of the varactor in the upper layer of the lower region of the semiconductor substrate.

[c21] 21.The method of claim 16, further comprising forming at least one isolation region adjacent to the lower, middle, and upper regions of the semiconductor substrate.

[c22] 22.The method of claim 16, further comprising forming at least one reach-through implant in electrical communication with the lower region of the semiconductor substrate.

[c23] 23.The method of claim 16, further comprising forming a silicided layer on a top of the semiconductor substrate above the upper region.